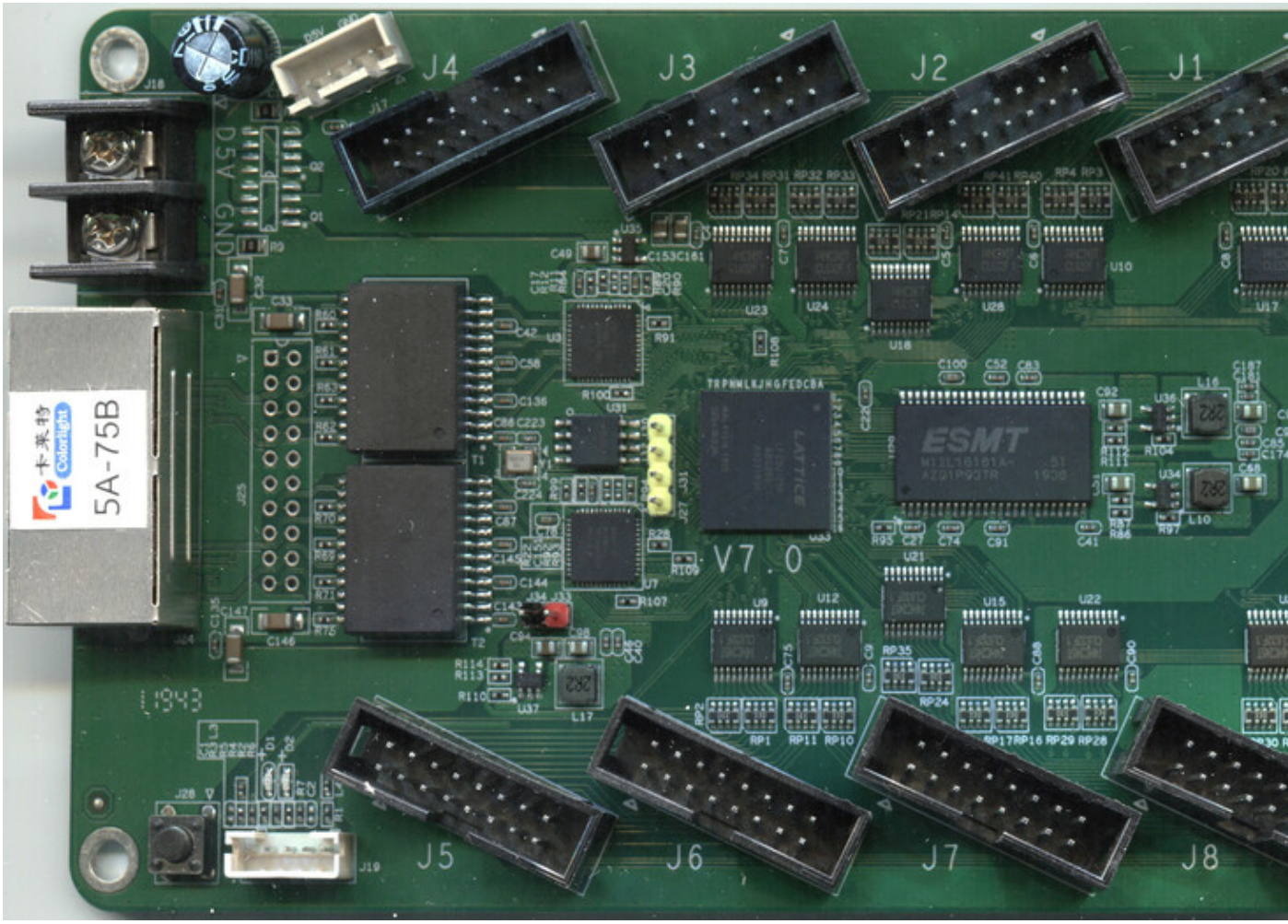
t=0x87d6bc0 [0,0]

Contents: [Dobrica PavlinuÅ¡iÄ 's random unstructured stuff]

Board version: v7.0

- Lattice ECP5 `LFE5U-25F-6BG256C` (product page)
- Winbond `25Q32JVSIQ`, 32 Mbits SPI flash (datasheet)
- 2x Broadcom `B50612D` Gigabit Ethernet PHYs (datasheet)
- 2x ESMT `M12L16161A-5T` 1M x 16bit 200MHz SDRAMs (organized as 1M x 32bit) (datasheet)
- 12x `74HC245T` Octal Bidirectional Transceiver (used for level translation to 5V)



links

- https://hackaday.com/2020/01/24/new-part-day-led-driver-is-fpga-dev-board-in-disguise/

chubby75

- https://github.com/q3k/chubby75/tree/master/5a-75b
  - upstream: https://github.com/tomverbeure/chubby75/tree/5a-75b/5a-75b
  - upstream for v7 board: https://github.com/miek/chubby75/blob/5a-75b-v7_pinout/5a-75b/hardware_V7.0.md

original protocol

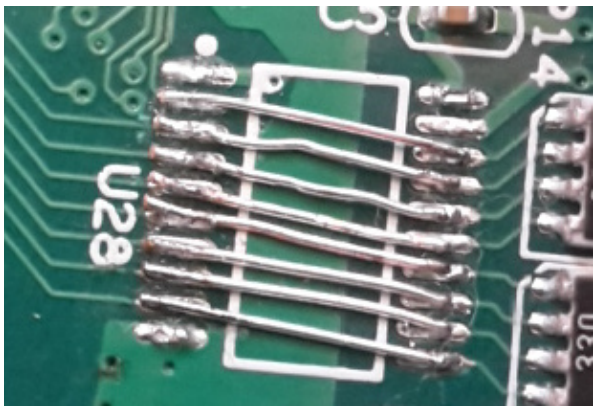
- send data to original fpga image: https://github.com/FalconChristmas/fpp/blob/master/src/channeloutput/ColorLight-5a-75.cpp

replace level shifters to get input

- https://twitter.com/edu_arana/status/1231466891354525698

https://twitter.com/Claude1079/status/1231194849350647808

SN74CBT3245APW 8bit bidirectional FET switches
QS3245QG



chiselwatt

https://github.com/antonblanchard/chiselwatt/commit/5a7fcbc8142ed2b390e1f8bfaaa801fe09a60351

UART RX is on J19, labelled key+ on the silk screen on the back
UART TX is on J1, pin 1.

LOCATE COMP "clock" SITE "P6";

LOCATE COMP "io_tx" SITE "F3";
LOCATE COMP "io_rx" SITE "M13";

litex

basic example of litex on colorLight 5A-75B based on fpga_101/lab004

- https://github.com/trabucayre/litexOnColorlightLab004/
- https://github.com/NiklasFauth/colorlight-led-cube
- https://github.com/ghent360/riscvOnColorlight-5A-75B

fpga pin mapping

https://twitter.com/adamgreig/status/1297255957320421383

I don't want to load a new image onto this totally blind, so I used the prjtrellis tools (https://github.com/YosysHQ/prjtrellis/) to write a script (https://github.com/adamgreig/cl/blob/master/pins.py) which works out input/output/bidi for all pins used in any ECP5 bitstream. It found only one unused pin...

https://github.com/adamgreig/cl/blob/master/pins.py

fpga images

- https://github.com/suglover/5a-75x-images
- ecpprog (FTDI jtag probe): https://github.com/gregdavill/ecpprog